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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,990	02/11/2004	Back-Won Lee	21C-0113	8230

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EXAMINER

TANG, MINH NHUT

ART UNIT PAPER NUMBER

2829

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/777,990	LEE, BACK-WON	
	Examiner	Art Unit	
	Minh N. Tang	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 11 February 2004.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 9-20 is/are rejected.
- 7) ☒ Claim(s) 8 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 February 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Drawings***

2. The drawings are objected to because "ANUPPER" in step S12 of Fig. 9 should be -- AN UPPER --. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

3. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

***Claim Objections***

4. Claims 1, 12-14 and 18 are objected to because of the following informalities:

a/ in claim 1, line 8, "first inspection line" should be -- first inspection signal --.

b/ in claim 12, line 1, "the input line is" should be -- the input lines are --.

c/ in claim 13, line 2, "the input line" should be -- the input lines --.

d/ in claim 14, line 1, "comprises" should be -- comprise --.

e/ in claim 18, line 10, "the input line" should be -- an input line --.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimada et al. (U.S.P. 5,576,730).

As to claim 1, Shimada et al. disclose, in Fig. 1, a mother substrate (22) comprising: a plurality of display cells (i.e., rows defined by a plurality of gate lines 1, hereinafter cells), each of the display cells (cells) having an inspection line (i.e., leftmost lines connecting to the gate driving circuit 5, hereinafter connecting lines) receiving a

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first inspection signal (GND, VDD, CLK, START) externally provided (see column 6, lines 54-58), a driving part (5) outputting a second inspection signal (Y1, Y2, ..., Yn) in response to the first inspection signal (GND, VDD, CLK, START) provided through the inspection line (connecting lines), and a pixel part (i.e., defined by boundary gate line 1 and data line 2) being driven in response to the second inspection signal (Y1-Yn); and an inspecting pad part (see the ends of the connecting lines, hereinafter, pads) extended from the inspection line (connecting lines) so as to provide the first inspection signal (GND, VDD, CLK, START) to the inspection line (connecting lines).

As to claim 2, Shimada et al. disclose in Fig. 1, the pixel part (defined by boundary gate line 1 and data line 2) comprises a plurality of pixels (i.e., defined by two adjacent gate lines 1 and data lines 2), each of the pixels having a gate line (1), a data line (2) substantially perpendicular to the gate line (1) and a switching device (4) connected to the gate and data lines (1, 2).

As to claim 3, Shimada et al. disclose in column 6, lines 54-58, the driving part (5) comprises a shift register having a plurality of stages (i.e., for sequentially sending signals Y1-Yn) so as to output the second inspection signal (Y1-Yn) to the gate line (1).

As to claim 4, Shimada et al. disclose in Fig. 1, the first inspection signal (Y1-Yn) has a voltage level (GND, CDD) suitable for substantially simultaneously driving the stages.

As to claim 5, Shimada et al. disclose in Fig. 1, the inspection line (connecting lines) comprises: a plurality of input lines (i.e., right part of the connecting lines) connected to the driving part (5) and spaced apart from each other in a predetermined

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distance; and a connecting line (i.e., left part of the connecting lines) electrically connected between the input lines and the inspecting pad part (pads).

As to claim 6, Shimada et al. disclose in Fig. 1, the input lines (right part of the connecting lines) comprise a start signal input line (i.e., line connecting to START signal), a clock input line (i.e., line connecting to CLK signal) and a driving voltage input line (i.e., lines connecting to GND, VDD signals) so as to receive signals used to drive the driving part (5).

As to claim 7, Shimada et al. disclose in Fig. 1, the start signal input line (line connecting to START signal) is connected to a first stage of the stages.

As to claim 9, Shimada et al. disclose in Fig. 1, the driving voltage input line (lines connecting to GND, VDD signals) receives a ground voltage (GND).

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 10-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim (U.S.P. 6,781,403).

As to claim 10, Kim discloses, in Figs. 1 and 2, a substrate (1) for a display panel, comprising: a lower substrate (2) having an inspection line (26) receiving a first inspection signal (i.e., gate driving signals) externally provided (see column 2, lines 61-

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64), a driving part (16) outputting a second inspection signal (i.e., scanning signal) in response to the first inspection signal (gate driving signals) provided through the inspection line (26), and a pixel part (i.e., defined by boundary gate lines 20 and data lines 18) being driven in response to the second inspection signal (scanning signal); and an upper substrate (4) being coupled to the lower substrate (2).

As to claim 11, Kim discloses in Fig. 1, the inspection line (26) comprises a plurality of input lines (28) spaced apart from each other in a predetermined distance; and a connecting line (22) electrically connected between the input lines (28).

As to claim 12, Kim discloses in Fig. 1, the input lines (28) are disposed on an edge of the lower substrate (2).

As to claim 13, Kim discloses in Fig. 1, the lower substrate (2) is partially grinded (i.e., after the inspection is complete), the input lines (28) disposed on the edge and a portion of the connecting line (22) disposed on the edge are removed while the lower substrate (2) is grinded (i.e., outer edge of the lower substrate 2 is cut for providing a display device).

As to claim 14, Kim discloses in Fig. 2, the input lines (28) comprise a start signal input line (for providing a gate start pulse GSP), a clock input line (for providing a gate shift clock signal GSC) and a driving voltage input line (for providing voltage signals Vcom, VGL, GND).

As to claim 15, Kim discloses in Fig. 2, the driving voltage input line (for providing voltage signals Vcom, VGL, GND) has a width wider than those of the start signal input line (for providing a gate start pulse GSP) and clock input line (for providing a gate shift

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clock signal GSC).

As to claim 16, Kim discloses in Figs. 1 and 2, the driving voltage input line (for providing voltage signals Vcom, VGL, GND) receives a first inspection signal (gate driving signal) externally provided, and provides the first inspection signal (gate driving signal) to the inspection line (26).

As to claim 17, Kim discloses in column 2, lines 37-41, a liquid crystal layer disposed between the lower substrate (2) and the upper substrate (4).

As to claim 18, Kim discloses, in Figs. 1 and 2, a method of manufacturing a display panel (21), comprising: fabricating a substrate (1) for a display panel (21), the substrate (1) having a lower substrate (2) and an upper substrate (4) coupled to the lower substrate (2), the lower substrate (2) having an inspection line (26) receiving a first inspection signal (gate driving signal) externally provided, a driving part (16) outputting a second inspection signal (scanning signal) in response to the first inspection signal (gate driving signal) provided through the inspection line (26), and a pixel part (21) being driven in response to the second inspection signal (scanning signal); providing the first inspection signal (gate driving signal) to the inspection line (26) to inspect the driving part (16) and pixel part (21); and insulating the inspection line (26) from an input line (28) to complete the display panel (21).

As to claim 19, Kim discloses in Fig. 1, fabricating a mother substrate (2) for the lower substrate (2) having an inspecting pad part extended from the inspection line (26); providing the first inspection signal (gate driving signal) to the inspecting pad part to inspect the mother substrate (2) for the lower substrate (2); fabricating a mother



substrate (4) for the upper substrate (4); combining the mother substrate for the lower substrate (2) with the mother substrate for the upper substrate (4); and cutting the combined substrate to complete the substrate for the display panel (21).

As to claim 20, Kim discloses in Fig. 1, the inspection line (26) is removed by grinding (i.e., cut to form a display device) an edge of the substrate for the display panel (21).

### ***Allowable Subject Matter***

9. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 8 recites, inter alia, the clock input line comprises a first clock input line that receives a first clock and a second clock input line that receives a second clock.

The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include the above limitations.

### ***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Tomita	US 2003/0030464 A1	Testing Method For Array Substrate.
Park	US 2002/0084965 A1	Liquid Crystal Display Device.
Kim et al.	6,839,121	Liquid Crystal Display Device Formed On Glass Substrate Having Improved Efficiency.


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Misawa et al.          5,754,158          Liquid Crystal Device.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor R. Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
MINH NHUT TANG  
PRIMARY EXAMINER  
4/28/05